REMARKS

This substitute specification is provided to overcome the rejections in the office communication and to bring this application to allowance. It is a substitution replacing the response forwarded September 9, 08.

In this substitute there are no amendments to the claims. Applicants are showing herewith the allowability of the claims. More particularly it will show that the claims as presented in response to the non-final office action indeed comply with the enablement requirement.

These remarks follow the order of the paragraphs of the office action dated July 9, 2008. Relevant portions of the office action are shown indented and italicized.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:
The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-10, 17-18, 21-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.
Claim 1 recites a "buffer storing indications of events" in line 2, "said apparatus for transferring interrupts from the peripheral device to a host computer" in lines 9-10, "moving the contents of the buffer to the payload portion of the control data block, and sending the control data block to the host computer system" in lines 18-19. The recitations suggest that indications of events are stored in the buffer and that the

indications of events (the contents of the buffer) are moved to a payload portion of the control data block and sending the control data block to the host computer system. The recitations also suggest that only interrupts from the indications of events (i.e. not the indications of events) are transferred from the peripheral device to the host computer system. It appears that the specification only discloses transferring all indications of events in the control block to the host computer.

In response, the applicants respectfully states that applicants show below that the claims are enabled by the description in the specification. This overcomes the rejection under 35 U.S.C. 112, first paragraph. Applicants maintain that the claims protect the embodiment in Figure 17 of the specification. This is based on the description of Figure 17 commencing on line 10 of page 38 in the specification as applied to the general invention description.

The description of Figure 17 reads:

"In preferred embodiments of the present invention, LCP interrupts 1590 are preprocessed in the interests of reducing processing burden on the software in the host 10. LCP interrupt information is written into the memory 60 of the host 10 to reduce software latency from repeated accesses by the ISOC 120. The generation of a new interrupt indication by each LCP channel is deferred until handling of previous channel interrupts is completed. The processing of LCP interrupts will now be described in detail with reference to Figure 17.

Referring now to Figure 17, an interrupt flow between the ISOC 120 and the host 10 comprises, at step 1600, either a software application 1610 in the transmission direction or the RX processor 160 in the reception direction setting a CompletionEventRequest bit in a descriptor 1620 for which an interrupt is required. The descriptor 1620 is stored in a descriptor queue 1630. At step 1640, once processing of the descriptor is completed, a completion event indication 1650 is sent to an interrupt FIFO buffer 1660 in the ISOC 120 by an interrupt controller of the ISOC 120. An EventMask bit is set in the LCP context 140. Completion event indications are queued in the interrupt FIFO 1660. At step

1670, when preset conditions are met, an Interrupt Control Block (ICB) 1680 is generated by the ISOC 120 from the information stored in the interrupt FIFO 1660. The preset conditions will be described shortly. At step 1690, the ICB 1680 is transferred to the memory 60 of the host 10. ICBs 1680 from the ISOC 120 are stored in a wrapped queue 1700 in the memory 60 of the host 10. At step 1710, an interrupt handler 1720 in the software of the host 10 reads the ICB 1680. At step 1730, the interrupt handler 1720 sends the completion event 1650 from the ICB 1680 to the application 1610. At step 1750, the application 1610 writes a ClearEventMask bit to the Doorbell register of the LCP channel to enable interrupts from the channel.

An active LCP channel can generate one or more completion events 1650 during operation. A completion event 1650 is generated when processing of the descriptor 1620 on which the CompletionEventRequest bit is set is completed. The operation of the ISOC 120 following a completion event varies depending on the value of the EventMask and the CompletionEvent bit in the context 140. If the EventMask bit is cleared, an indication is sent to the interrupt controller of the ISOC 120 and the EventMask bit is set by the ISOC 120. If the EventMask bit is set and the CompletionEvent bit in the channel's context 140 is cleared, no indication is transferred to the interrupt controller and the CompletionEvent bit is set by the ISOC 120. If the EventMask bit and the CompletionEvent bit in the channel's context 140 are both set, no action is taken. The EventMask bit is cleared at channel initialization. It is also cleared after the ClearEventMask bit is written to the context 140 of the channel via the Doorbell register. If the CompletionEvent in the channel's context 140 is set and the mask bit is cleared by the ClearEventMask bit in the Doorbell register, an indication of the event completion is sent to the interrupt controller and the CompletionEvent bit is cleared. The completion events are logged in the FIFO 1660 by the interrupt controller. Each entry in the FIFO 1660 holds a field for describing the number of the LCP channel generating the event."

Claim 1 is copied below showing correspondence of the specification described components [shown with a double underline] as described in Figure 17, etc., following each corresponding elements of the claim.

Claim 1. An apparatus Figure 17 comprising:

a buffer 1700 for storing indications of events generated by a plurality of ports 140 of a peripheral device 80 in Figures 1,2,3, 12 &14, events include at least one of any of the following: an interrupt; an internal flag; a status indication of completion of the read operation; an indication that a new header is waiting; an indication that a packet header is ready; an indication triggered at an end of header processing, a descriptor, or a set of descriptors; a completion indication as a received packet which includes an acknowledgment; an indication of reception of a frame for transmission; an indication that a EventMask bit is cleared, an indication that the EventMask bit is cleared; an indication that a predetermined minimum number of event completed, said apparatus for transferring interrupts from the peripheral device to a host computer system, and

a controller 120 [includes context 140] having a preset condition for an application, said preset condition comprising one of: a determination that the buffer 1700 is full; a determination that at least a predetermined plurality of indications is stored in the buffer 1700; a predetermined period has elapsed; and a determination that at least one indication is stored in the buffer 1700 and that a predetermined period has elapsed, said controller 120 for, in response to a preset condition being met based on said indications, generating a control data block 1680, & Fig. 18 comprising a payload portion having a plurality of fields each corresponding to a port LCP# fields in Fig,. 18 from said plurality of ports 140 & 100 in Fig. 3 and a header portion WORD 0 in Fig. 18 having an identifier INDEX/CNT field in Fig. 18 for identifying the control data block 1680 & Fig. 18 moving the contents of the buffer 1660 to the payload portion of the control data block 1680 and sending the control data block 1680 to the host computer system via one a predesignated port of the plurality of 100 inside 110 in Fig 3 .

The controller, preset condition, indications stored in the buffer; a predetermined period has elapsed; a determination that a predetermined period has elapsed, a control data block, payload portion, plurality of fields, header portion having an identifier for identifying the control data block, are all enabled by the first paragraphs of the description of the invention, which read:

> "The present invention provides methods, systems and apparatus for transferring interrupts from a peripheral device to a host computer system. An example of apparatus comprises: a buffer for storing indications of interrupts generated by the peripheral device; and a controller for, in response to a preset condition being met, generating a control data block having a payload portion, moving the contents of the buffer to the payload portion of the control data block, and sending the control data block to the host computer system. The buffer preferably comprises a first in - first out memory buffer
>
> Preferably, the preset condition comprises a determination that the buffer is full. The preset condition may comprise a determination that at least a predetermined plurality of indications is stored in the buffer and that a predetermined period has elapsed. Similarly, the preset condition may comprise a determination that at least one indication is stored in the buffer and that a predetermined period has elapsed."

Thus, claim 1 is entirely enabled by the specification and protects the embodiment of Figure 17. This overcomes the rejection of Claims 1-10, 17-18, 21-22 under 35 U.S.C. 112, first paragraph, which are allowable.

> *4. Claims 11-16, 19-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.*
>
> *It appears that there is no support for "moving the contents of the buffer to the corresponding fields of the payload portion" - as page 38, lines 25-26 merely discloses "when preset conditions are met, an Interrupt Control Block (ICB) 1680 is generated by the ISOC 120 from the information stored in the interrupt FIFO 1660".*

In response, the applicants respectfully states that the Claims 11-16, 19-20 also protect the embodiment of Figure 17 and are enabled in the specification and the paragraphs copied above. The description of the embodiment of Figure 17, enables Claims 11-16, 19-20 and overcomes the rejection under 35 U.S.C. 112, first paragraph.

> *5. Claims 13-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.*
>
> *Claim 13 recites "at least a predetermined plurality of indications is stored in the buffer". Claim 14 recites "at least one indication is stored in the buffer". Claim 15 recites "a count indicative of the number of indications included in the payload portion".*
>
> *Claim 1 suggests storing only interrupts in the buffer and does not suggest storing indications other than interrupts in the buffer. The claims suggest that interrupts and indications are two different entities, while the specification only discloses only one entity being stored in the buffer and the count being indicative of only one entity.*

In response, the applicants respectfully states that the description provided above regarding claim 1 is applicable to overcome the rejections of claims 13-15 under 35 U.S.C. 112, first paragraph.

> *6. Claims 10, 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.*
>
> *The examiner cannot find support for the limitations of the claims. In particular, it is not clear what constitute the claimed apparatus, the claimed host processing system, the claimed memory of the host processing system, the claimed data processing system, the claimed host computer, and the claimed memory of the host computer system. Applicant is required to specifically point out where to find the support for the limitations of the claims in the specification, by page and line number - and in particular, applicant is required to map out each of the elements claimed with the teachings of the specification.*

In response, the applicants respectfully states that the description provided above regarding claim 1 is applicable to overcome the rejections of claims 10 and 22 under 35 U.S.C. 112, first paragraph.

7. No art rejection was made to claims 1-16, 21-22 because the scope of the claims is ambiguous, and it is not possible for the examiner to apply prior art without making a great deal of speculation.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless — (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Raasch et al. (US 5,333,273).

In response, the applicant respectfully states that Claims 17-20 are not made patentable by the invention of Raasch. The present invention, claimed in Claims 17-20, provides:

"Methods, systems and apparatus for transferring interrupts from a peripheral device to a host computer system is described. In an example embodiment, an apparatus comprises a buffer for storing indications of interrupts generated by the peripheral device. In response to a preset condition being met, a controller generates a control data block having a payload portion, moves the contents of the buffer to the payload portion of the control data block, and sends the control data block to the host computer system."

Whereas, the cited art to Raasch, US Patent 5,333,273, filed: September 3, 1992, is entitled: "Protected hot key function for microprocessor-based computer system". The abstract reads: "An ISA-compatible computer system includes an additional function key on its keyboard. The additional function key does not have a defined function for conventional ISA-standard computers. When a conventional alphanumeric key or function key is activated on the keyboard, the computer system is interrupted using IRQ1 and the key information is communicated to the computer system so that the computer system can respond in a conventional manner using a conventional keyboard interrupt handling routine. When the additional function key and an alphanumeric key are activated in combination, a second interrupt different from the IRQ1 interrupt is activated (e.g., IRQ15). The computer system responds to the second interrupt by

inputting an identification of the activated alphanumeric key and performing a selected predetermined function in response thereto. The handling of the second interrupt is performed by a separate interrupt handling routine within the computer system so that conventional terminate and stay resident (TSR) programs that intercept conventional keyboard inputs cannot readily intercept keyboard input initiated by the additional function key ".

Thus Raasch is not concerned with or teach. indications of events or a preset condition as in the claims. In particular, Raasch et al., is not prior art because Raasch operates in a different domain: Keyboard attached via ISA. Raasch solves a different problem, to : Adding a capability to invoke multiple TSRs from the keyboard. The presently claimed invention operates in the domain of an I/O attached adapter (e.g. Network Adapter), and the claims are directed to improve the system overhead that is associated with interrupts.

Examples of words that exclude Raasch as prior art include:

buffer for storing indications of events generated by a plurality of ports,

an indication that a packet header is ready,

indication triggered at an end of header processing,

an indication that a EventMask bit is cleared, and

a predetermined period has elapsed.

Thus, all claims are allowable over Rausch.

10. As per claims 17, 19, Raasch teaches a computer program product (or article of manufacture) comprising a computer usable medium [138, FIG. 1] having computer readable program code means [BIOS: col. 5, lines 18-21] embodied therein for causing transfer of interrupts [col. 4, lines 66-68], the computer readable program code means in said computer program product (or article of manufacture) comprising computer readable program code means [BIOS: col. 5, lines 18-21] for causing a computer (100, FIG. 1] to effect the functions of the apparatus of claim 1 (or the method of claim 11)- as the BIOS would cause a computer to effect the functions of any apparatus, hence including functions of the apparatus of claim 1; and as the BIOS would cause a computer to effect the steps of any method, hence including the steps of the method of claim 11.

11. As per claim 18, Raasch teaches a computer program product comprising a computer usable medium [138, FIG. 1] having computer readable program code means [BIOS: col. 5, lines 18-21] embodied therein for causing data processing [col. 5, lines 18-31],

the computer readable program code means in said computer program product comprising computer readable program code means [BIOS: col. 5, lines 18-21] for causing a computer [100, FIG. 1] to effect the functions of the apparatus of claim 10 - as the BIOS would cause the computer to effect the functions of any apparatus, hence including the functions of the apparatus of claim 10.

12. As per claim 20, Raasch teaches a program storage device [138, FIG. 1] readable by machine [100, FIG. 1], tangibly embodying a program of instructions [BIOS: col. 5, lines 18-21] executable by the machine to perform method steps for transferring interrupts [col. 4, lines 66-68], said method steps comprising the steps of claim 11 (the BIOS would cause a computer to effect the steps of any method, hence including the steps of the method of claim 11).

In response, the applicants respectfully states that Raasch is not concerned with or teach. indications of events or a preset condition as in the claims. The cited Raasch portion col. 5, lines 18-21 reads:

> The keyboard interrupt service routine may be located in the RAM 120 or it may be located in the ROM 138. Generally, the keyboard interrupt service routine for the keyboard is provided as a basic operating function of the computer system 100 and is stored in the ROM 138 as part of the Basic Input/Output System (BIOS) of the computer system.

The cited Raasch portion col. 4, lines 66-68 reads:

> The interrupt controller 130, the DMA controller 132 and the interface circuitry 134 provide communications between the processor bus 114 and an ISA bus 140.

This apparently fails to show the elements of claims 17-20. Thus, all claim 17-20 are allowable.

Response to Arguments

13. Applicant's arguments filed February 19, 2008 have been fully considered but they are not persuasive.
A. With respect to the rejections of claims 1-10, 17-18, 21-22, applicant indicates that "a buffer storing indications of events" is recited on page 2, line 4. Page 2, line 4, however, recites "a buffer for storing indications of interrupts". Note that "indications of interrupts" and "indications of events" do not have the same meaning.

B. With respect to the rejections of claims 11-16, 19-20, applicant indicates that "moving the contents of the buffer to the corresponding fields of the payload portion" is recited on page 44, line 10. While the recitation is found on page 44, line 10, the recitation is part of a claim that

does not have antecedent basis in the specification — as page 38, lines 25-26 merely discloses "when preset conditions are met, an Interrupt Control Block (ICB) 1680 is generated by the ISOC 120 from the information stored in the interrupt FIFO 1660".

C. With respect to the rejections of claims 13-15, applicant indicates the recitations are found on page 5, line 2; page 5, line 4; and page 5, line 7. The examiner found the recitations on pages, lines 4-5; page 5, lines 6-7; and pages, lines 9-10 instead. While the recitations can be found, the specification suggests storing only interrupts in the buffer and does not suggest storing indications in the buffer. The claims suggest that interrupts and indications are two different entities, while the specification only discloses only one entity being stored in the buffer and the count being indicative of only one entity (the one entity being interrupts).

D. With respect to the rejections of claims 10 and 22, applicant does not adequately provide support for the claimed elements requested by the examiner.

E. With respect to the art rejections of claims 17-20, applicant argues that Raasch is not concerned with or teach indications of events or a preset condition as in the claims. Raasch was not relied upon to teach indications of events or a preset condition, because the claims do not require such limitations. Applicant appears to misinterpret the rejections.

> *Claim 17 only requires a program code means for causing transfer of interrupts, and a program code means for causing a computer to effect all functions of the apparatus of claim 1. Claim 18 only requires a program code means for causing a computer to effect all functions of the apparatus of claim 10. Claim 19 only requires a program code means for causing transfer of interrupts, and a program code means for causing a computer to effect all steps of the method of claim 11. Claim 20 only requires a program of instructions to perform method steps for transferring interrupts, the method steps comprising steps of the method steps of the method of claim 11.*
>
> *Raasch teaches a BIOS and transfer of interrupts (col. 4, lines 66-68; col. 5, lines 16-21). A BIOS would cause a computer to effect the functions of any apparatus (i.e. including the functions of applicant's apparatus), and because a BIOS would cause a computer to effect/perform the steps of any method (i.e. including the steps of applicant's methods).*

14. In addition, to help the examiner better understand the scope of the claimed invention and further the prosecution, the examiner requests that applicant identify - by reference to labels in

the drawings, and/or page and line numbers in the specification - the following elements and/or steps: elements: apparatus, buffer, indications of interrupts, plurality of ports, peripheral device, host computer system, controller (in claim 1); communications device (in claims 8-9); data communications network interface (in claims 9-10); host processing system, data processing system (in claim 10) steps: the apparatus transferring interrupts, moving the contents of the buffer to the payload portion of the control data block (claim 1); storing interrupts, moving the contents of the buffer to the corresponding fields of the payload portion (in claim 11).

In the interview dated June 16, 2008, applicant identifies the followings: Apparatus is ISOC 120 [FIG. 17] Buffer is FIFO 1660 [FIG. 17] Interrupts are indications of events (i.e. "indications of interrupts" are therefore meaningless) Plurality of ports can be logical or physical — but no identification of a plurality of ports for a peripheral device was made Peripheral device is device 20 [FIG. 1] Host computer system is any of Host 10 [FIG. 1], or Host 10 [FIG. 17] Controller is inherent for generating control data block [1680, FIG. 17] Communication device is network adapter 80 [FIG. 2] Data communication network interface is network adapter 80 [FIG. 2] Host processing system is CPU SO [FIG. 1] Data processing system is ISOC 120 [FIG. 2] A memory in line 2 of claim 10 may not be memory 60 [FIG. 1, FIG. 17] Data communication interface is network adapter 80 [FIG. 2] Data communication network is network 30 [FIG. 1] The above identifications cannot support the followings: An apparatus [120, FIG. 17] moving the contents of the buffer [1660, FIG. 17] to the payload portion of the control data block, and sending the control data block to the host computing system [10, FIG. 17] via one port of the plurality of ports — as FIG. 17 shows sending the control data block [1680] to the host computing system through memory [60, FIG. 17], i.e. not through a port of the plurality of ports (of the peripheral device 20 — FIG. 1] — see lines 18-20 of claim 1.

A data communication network interface [80, FIG. 2] comprising the communication device as claimed in claim 8 [i.e. communication device 80, FIG. 2] — see claim 9.

An apparatus [120, FIG. 17] comprising a host processing system [SO, FIG. 1] having a memory [not identified]...forming a data processing system [120, FIG. 17] for controlling flow of interrupts from the data communication interface [80, FIG. 2] to the memory of the host processing system because FIG. 1, FIG. 2 and FIG. 17 do not show the apparatus 120 comprising CPU SO — see claim 10.

The examiner is not quite sure what applicant intends to claim with the current claims. The examiner suggests that applicant maps the claims to the teachings of the disclosure, makes appropriate amendments, and requests an interview with the examiner to explain what is being claimed prior to filing a response to further prosecution of the application. Without understanding what applicant intends to claim, it is not possible for the examiner to properly examine the invention.

In response, the applicants respectfully states that in consultation with a primary inventor, applicants indicate that the claimed elements correspond to the specification description as provided in the response above.

It is anticipated that this brings claims to allowance, particularly claims 1-10, 17-18, 21-22. Please contact the undersigned if any question remains.

Please charge any fee necessary to enter this paper to deposit account 50-0510.

Respectfully submitted,

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